

(SYLLABUS)

1.

(Course Title)		(Instructor)			
(Year)	2024	(Semester)	2	(Course No.)	2150078701
(Class)	01	(Open to)	2, 3, 4	(Course Classification)	-
/	1.0 / 02 / 2		100	가	가
(Office)	704	(Telephone)	02-828-7489	(e-mail)	inchul.song@ssu.ac.kr
	(*) (ABEEK Classification)		(*) (ABEEK Requirement)		
(Course Description)	, Verilog				

(combinational & sequential logic circuit)	
Verilog-HDL programming	

가	(100)	(100%)
	100	20
	100	30
	100	40
	100	10

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(Required Texts)		* / PPT
	()	* /Digital Design: With an Introduction to the Verilog HDL, VHDL and System Verilog/M.Morris R. Mano, Michael D. C/Pearson/2017/6th
	ARTY-S7 FPGA	, Dual-7 Segment
	- 9/6 - 3 -	15:00~16:50

2.

(Week)	(Keyword)	(Description)		(Texts)
01	, Vitis-vivado	,	, , ,	
02	, Function Generator, DC		, , ,	
03	Vitis-vivado, Arty-S7, Spartan-7	, vitis-vivado	, , ,	
04	, , Verilog HDL		, , ,	,
05	Test bench, mux, demux,, Verilog-HDL	Test bench, mux, demux, RTL Analysis, Data flow, Behavioral modeling	, , ,	,
06	Decoder and encdoer	Decoder and encoder	, , ,	,
07	7 Segment, common anode, Common cathode	7 Segment driver	, , ,	,
08		가		1~7
09	D-Latch, D-Flip/Flop	D-Latch, D-F/F	, , ,	,
10	Register, multi-function Register		, , ,	,
11	FSM, Moore and Mealy State diagram	FSM	, , ,	,
12	Counter, Frequency divider, BCD(Binary coded decimal)		, , ,	,
13	System block diagram, mux, BCD to dual BCD, BCD to 7-segment	Two digit decimal counter	, , ,	,
14	Up/down counter	Up/down 2-digit counter	, , ,	,
15		가		9~14

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3. ()

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	Open-ended problem		
	Teamwork		
	Communication skills		